

**Form PTO-1449 (modified)**Atty. Docket No.  
ALTR:023Serial No.  
10/757,928

List of Patents and Publications for Applicant's

Applicant  
HUANG ET AL.**INFORMATION DISCLOSURE STATEMENT**

(Use several sheets if necessary)

Filing Date:  
1/15/04

Group:

2827

FEB 14 2005

U.S. Patent Documents  
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See Page 2**U.S. Patent Documents****U.S. Patent Documents**

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
MW	A1	4,281,398	7/28/81	McKenny et al.			2/12/80
MW	A2	US2002/01058 54A1	8/8/02	Huh et al.			1/23/02
MW	A3	US2003/02064 77A1	11/6/03	Waller et al.			5/22/03
MW	A4	US2004/00221 10A1	2/5/04	Haraguchi et al.			2/25/03
MW	A5	US2004/00278 93A1	2/12/04	Kurita			7/14/03
MW	A6	4,724,422	2/9/88	Golab			9/13/85
MW	A7	4,829,481	5/9/89	Johnson et al.			10/22/87
MW	A8	4,887,239	12/12/89	Turner			7/7/86
MW	A9	5,349,555	9/20/94	Nakajima			4/27/93
MW	A10	5,821,770	10/13/98	Rees			4/30/96
MW	A11	5,825,698	10/20/98	Kim et al.			10/30/97
MW	A12	6,020,777	2/1/00	Bracchitta et al.			9/26/97
MW	A13	6,205,050	3/20/01	Tamaki			12/9/99
MW	A14	6,215,173	4/10/01	Echigoya			11/12/99
MW	A15	6,215,715	4/10/01	Lee et al.			7/1/99
MW	A16	6,236,241	5/22/01	Liu et al.			4/12/00
MW	A17	6,404,264	6/11/02	Daniel et al.			12/6/99
MW	A18	6,600,686	7/29/03	Huh et al.			1/23/02
MW	A19	6,281,739	8/28/01	Matsui			7/6/99

Examiner: Michael Nenney

Date Considered: 3/10/2006

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(2/14/05 cont'd)

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**Foreign Patent Documents**

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Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

**Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)**

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Exam. Init.	Ref. Des.	Citation
w	C1	Ouellette et al., "Shared Fuse Macro For Multiple Embedded Memory Devices With Redundancy", IEEE Custom Integrated Circuits Conference, 2001, pps. 191-194.
w	C2	McCollum et al., "Reliability Of Antifuse-Based Field Programmable Gate Arrays For Military And Aerospace Applications", Actel Corporation, Abstract, September 2001, 6 pgs.
w	C3	Benedetto et al., "Amorphous Silicon Antifuse Programmable-Array-Logic Devices For High Reliability Space Applications", UTMC Microelectronic Systems, January 2002, 4 pgs.
w	C4	Laville et al., "Integrated Offset Trimming Technique", 27 <sup>th</sup> European Solid-State Circuits Conference, September 2001, 4 pgs.
w	C5	Actel, Reliability Considerations For Automotive FPGAs, White Paper, September 2003, 17 pgs.
w	C6	MRAM Redundancy Scheme (prior art available prior to filing date of the present application)

Examiner: Michael Weinberg | Date Considered: 3/10/2006

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